



THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. .... 09/559,903  
Filing Date .... April 26, 2000  
Inventor .... Zhiping Yin et al.  
Assignee .... Micron Technology, Inc.  
Group Art Unit .... 2815  
Examiner .... G. Eckert II  
Attorney's Docket No. .... MI22-1427  
Title: Circuitry and Gate Stacks

**SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT**

References -- See attached Form PTO-1449

In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the United States patents and other references listed on the attached Form PTO-1449.

No admission is made regarding whether all the submitted references are prior art.

This Supplemental Information Disclosure Statement is being filed after the filing of the Request for Continued Examination (RCE) Application and before receipt of the first Office Action. Therefore, no fee is believed to be required. However, in the event that a fee is required for filing this Supplemental Information Disclosure Statement, please charge the fee specified under 37 C.F.R. §1.17(p) to Deposit Account No. 23-0925. Please credit Deposit Account No. 23-0925 with any overpayment of the above fee.

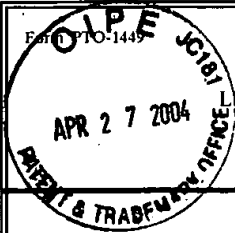
Citation of these references is respectfully requested.

Respectfully submitted,

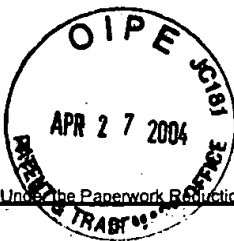
Date:

*April 27 2004*

*Jennifer J. Taylor*  
Jennifer J. Taylor, Ph.D.  
Reg. No. 48,711

		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. M122-1427		SERIAL NO. 09/559,903		
		LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Zhiping Yin et al.		
						FILING DATE April 26, 2000		GROUP 2815
U.S. PATENT DOCUMENTS								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	AA	4,971,655	11-1990	Stefano et al.				
	AB	6,498,084 B2	12-2002	Bergemont				
	AC	5,036,383	07-1991	Mori				
	AD							
	AE							
	AF							
	AG							
	AH							
	AI							
	AJ							
	AK							
	AL							
FOREIGN PATENT DOCUMENTS								
		Document Number	Date	Country	Class	Subclass	Translation	
							Yes    No	
	AM	08-045926A	02-1996	Japan (abstract only)				
	AN	JP8051058	02-1996	Japan (abstract only)				
	AO	JP63316476	12-1988	Japan (abstract only)				
	AP	JP8078322	03-1996	Japan (abstract only)				
	AQ							
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)								
	A R		Stanley Wolf, SILICON PROCESSING FOR THE VLSI ERA, Vol. 3, Lattice Press 1995, page 635.					
	AS							
EXAMINER			DATE CONSIDERED					
<p>*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.</p>								

EL 979979042



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PTO/SB/21 (03-03)

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<b>TRANSMITTAL FORM</b>  (to be used for all correspondence after initial filing)	Application Number	09/559,903
	Filing Date	April 26, 2000
	First Named Inventor	Zhiping Yin
	Art Unit	2815
	Examiner Name	G. Eckert II
Total Number of Pages in This Submission	Attorney Docket Number	MI22-1427

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Signature	<i>Jennifer J Taylor</i>
Date	April 27, 2004

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